The M88000 RISC Family

In Brief . . .

Motorola's 88000 Family comes from the only company committed to long–term upward software compatibility through such features as hardware interlocked and protected pipelines. Our goal is to make sure each generation of the 88000 RISC family delivers a high performance level while maintaining software compatibility.

Motorola's 88000 RISC Microprocessors

. . . a performance architecture

Architecture, Performance, and Software Compatibility

The 88000 RISC was designed from the start for superscaler implementations. In fact, the design of the second generation 88110 microprocessor is a unique superscaler implementation called Symmetric Superscalar™. The Symmetric Superscaler design allows you to execute multiple instructions in a single clock cycle without any restrictions on instruction ordering. So there are no wait states or performance penalties because of out of order instructions.

Also, while other RISC microprocessors may be limited in the instructions they can execute in a single clock cycle, members of the 88000 are able to execute multiple instructions per clock cycle, thus providing the performance edge required for next generation system designs.

Performance Plus Software Compatibility

Although high performance is recognized as a key feature for systems design, software compatibility is also important. Motorola's 88000 Family comes from the only company committed to long term upward software compatibility through such features as hardware interlocked and protected pipelines. Our goal is to make sure each generation of the 88000 RISC family delivers a high performance level while maintaining software compatibility. This gives the opportunity for designing one of the industry's highest performance systems, while leveraging your largest dollar investment in new systems, your software.

Software compatibility is also promoted through standards to provide an open systems environment benefitting system companies, software developers, and end users because 88000 based systems from different vendors will run all of the same software.

Microprocessors

MC88100RC
32–Bit RISC Microprocessor

The MC88100 is the first processor in the 88000 Family of RISC (reduced instruction set computer) microprocessors. Implemented with Motorola's HCMOS technology, the MC88100 incorporates 32–bit registers, data paths, and addresses. In designing the MC88100, Motorola has incorporated a high degree of fine–grain parallelism; four independent execution units maintain separate, fully concurrent execution pipelines. Most instructions operate in one machine cycle or effective concurrent execution can be accomplished through internal pipelines in one machine cycle.

A common register file provides data sharing and synchronization control among the execution units through register scoreboarding.

The MC88100 addresses a variety of applications requiring high operational speeds and efficient, fast–execution architectures. All data manipulation instructions are nondestructive register to register or register with immediate operations, allowing both fast operand access and operand reuse. IEEE 754 floating–point arithmetic is supported in the processor. Instruction and data memory space are accessed through separate memory ports, allowing simultaneous access to dedicated memory areas. The 88000 Family includes the MC88200 CMMU (cache/memory management unit), which adds high–speed memory caching, two–level, demand–paged memory management, and support for shared–memory multiprocessing. The 88000 Family also includes a full line of highly optimizing compilers, operating systems, development boards, and development tools.

MC88110RC
32–Bit RISC Microprocessor

The MC88110 is the second implementation of the 88000 family of reduced instruction set computer (RISC) microprocessors. The MC88110 is a Symmetric Superscalar machine capable of issuing and retiring two instructions per clock without any special alignment, ordering, or type restrictions on the instruction stream. Instructions are issued to multiple execution units, execute in parallel, and can complete out of order, with the machine automatically keeping results in the correct program sequence. The Symmetric Superscalar design allows sustained performance to approach the peak performance capability.

The MC88110 uses dual instruction issue and simple instructions with extremely rapid execution times to yield maximum efficiency and throughput for 88000 systems. Instructions either execute in one clock cycle, or effective one clock cycle execution is achieved through internal pipelining. Ten independent execution units communicate with a general register file and an extended register file through multiple 80–bit internal buses. Each of the register files has sufficient bandwidth to supply four operands and receive two results per clock cycle. Each of the pipelined execution units, including those that execute floating–point and data movement instructions, can accept a new instruction and retire a previous instruction on every clock cycle.

In a single chip implementation, the MC88110 integrates the central processing unit, floating point unit, graphics processing unit, virtual memory address translation, instruction cache, and data cache. The MC88110 maintains compatibility with MC88100 user application software.

Cache/Memory Management Units

MC88200RC

16–Kilobyte Cache/Memory Management Unit (CMMU)

The MC88200 CMMU is a high–performance, HCMOS VLSI device providing zero–wait–state memory management and data caching. The MMU (memory management unit) efficiently supports a demand–paged virtual memory environment with two logical address ranges (user/supervisor) of 4 gigabytes each. Translated addresses are provided by one of two ATCs (address translation caches), providing address translation in one clock cycle for most memory accesses. The PATC (page address translation cache) is a 56–entry, fully associative cache containing recently used translations for 4–kilobyte memory pages and is maintained by MC88200 hardware. The BATC (block address translation cache) is a 10–entry cache, loaded by software, containing translations for 512–kilobyte memory blocks. The BATC translations are used for operating system software or for other memory–resident instructions and data. In addition, the MMU provides access control for the two logical address spaces. The CMMU data cache is a 16–kilobyte, four–way, set–associative cache for instruction or data storage. The cache incorporates memory–update policies and cache–coherency mechanisms that support multiprocessor applications. The MC88200 CMMU also includes an MC88100–compatible P bus (processor bus) interface and an M bus (memory bus) interface. A processor may use two or more CMMUs for increased data cache and ATC sizes.

MC88204RC

64K–Byte Cache/Memory Management Unit (CMMU)

The MC88204 CMMU is a high–performance, HCMOS VLSI device providing zero–wait–state memory management and data caching. The memory management unit (MMU) efficiently supports a demand–paged virtual memory environment with two logical address ranges (user/supervisor) of 4 Gbytes each. Translated addresses are provided by one of two address translation caches (ATCs), providing address translation in one clock cycle for most memory accesses. The page address translation cache (PATC) is a 56–entry, fully associative cache containing recently used translations for 4K–byte memory pages and is maintained by MC88204 hardware. The block address translation cache (BATC) is a 10–entry cache, loaded by software, containing translations for 512K–byte memory blocks. The BATC translations are used for operating system software or for other memory–resident instructions and data. In addition, the MMU provides access control for the two logical address spaces. The CMMU data cache is a 64K–byte, four–way set–associative cache for instruction or data storage. The cache incorporates memory–update policies and cache–coherency mechanisms that support multiprocessor applications. The MC88204 CMMU also includes an MC88100–compatible processor bus (P bus) interface and memory bus (M bus) interface.

The MC88204 CMMU is completely software and pin–level compatible with the MC88200 16K–byte CMMU. The functionality of the MC88204 is identical to that of the MC88200. With board layout constraints in mind, a central processing unit (CPU) may use up to two MC88204 CMMUs on the data P bus and up to two MC88204 CMMUs on the instruction P bus to increase data cache and ATC sizes.

MC88410

Secondary Cache Controller

The MC88410 is a highly integrated secondary cache controller for the MC88110 microprocessor that reduces memory latency and extends multiprocessing capability for those seeking the highest level of system performance. Used with the MCM62110 Fast Static RAM, it provides a functionally complete secondary cache solution for both uniprocessor and multiprocessor environments. The MC88410 provides tag, control and buffering for 1/4, 1/2, and 1 Mbyte secondary cache configurations, all in a single chip cache controller. The MC88410 eliminates external logic between the processor and the secondary cache, provides bus arbitration for the MC88110, and requires no external programming.

The MC88410 and MCM62110 are optimized to provide low latency memory access to the MC88110 processor. Initial accesses incur only one wait state. Subsequent transactions in a burst incur zero wait states. Data streaming to the processor reduces the penalty on secondary cache misses.

The MC88410 expands the MC88110's system flexibility by providing a choice of secondary cache line size, burst byte ordering, and system clock frequency. The MC88410 extends the MC88110 multiprocessing capability by significantly reducing system bandwidth consumption. This increased available bandwidth, along with the MC88410's hardware enforced cache coherency protocol, enable the implementation of dual bus systems and scalable shared–bus multiprocessing systems.